What Is Claimed Is:

1. A lock detector block for detecting whether an output clock signal is locked to an input reference signal, said lock detector block comprising:

a first sampling circuit receiving an up signal as an input and being clocked by a down signal, wherein said up signal indicates that the frequency of said output clock signal is to be increased and said down signal indicates that the frequency of said output clock signal is to be reduced to lock said output clock signal to said input reference clock signal, said first sampling circuit generating a first output indicating whether said output clock signal is out-of-lock;

a second sampling circuit receiving said down signal as an input and being clocked by said up signal, said second sampling circuit generating a second output indicating whether said output clock signal is out-of-lock; and

an examining circuit receiving said first output and said second output, and generating a signal indicating that said output clock signal is locked to said input reference signal if both said first output and said second output indicate that said output clock signal is not out-of-lock.

2. The lock detector block of claim 1, wherein said examining circuit comprises a NOR gate, said first sampling circuit comprises a first flip-flop and said second sampling circuit comprises a second flip-flop.

3. The lock detector block of claim 2, further comprising:

a first delay element placed before either a data input or a clock input of said first flip-

flop; and

a second delay element placed before either a data input or a clock input of said second flip-flop.

4. The lock detector block of claim 3, further comprises:

a plurality of flip-flops cascaded in series;

a first one of said plurality of flip-flops receiving said signal generated by said examining circuit as input, and wherein said plurality of flip-flops are clocked by an output of one of said first delay element and said second delay element; and

an OR gate generating an output by performing a logical OR operation on the outputs of said plurality of flip-flops cascaded in series,

wherein said output of said OR gate represents a jitter free indication of whether said output clock signal is locked to said input reference signal.

5. The lock detector block of claim 4, wherein said plurality of flip-flops cascaded in series are clocked by a delayed signal generated by either said first delay element or said second delay element.

6. The lock detector block of claim 5, wherein said up signal and said down signal are generated by a phase frequency detector based on a divided clock signal and said input reference signal, wherein said divided clock signal is generated by dividing said output clock signal.

7. An out-of-lock detector block for detecting whether an output clock signal is out-of-lock with an input reference signal, said out-of-lock detector block comprising:

an XOR gate receiving an up signal and a down signal,

wherein said up signal indicates that the frequency of said output clock signal is to be increased and said down signal indicates that the frequency of the said output clock signal is to be reduced to lock said output clock signal to said input reference clock signal,

wherein an output of said XOR gate represents whether said output clock is out-of-lock with said input reference signal.

8. The out-of-lock detector block of claim 7, further comprising:

a plurality of flip-flops cascaded in series;

a first one of said plurality of flip-flops receiving an output of said XOR gate as an input; and

a NAND gate receiving an output of each of said plurality of flip-flops,

wherein an output of said NAND gate generates a jitter free signal indicating whether said output clock signal is out-of-lock with said input reference signal.

9. The out-of-lock detector block of claim 8, wherein each of plurality of flip-flops cascaded in series is clocked by said output clock signal.

10. A lock generator circuit for generating a lock signal indicating whether an output clock signal is locked to an input reference signal, said lock generator circuit comprising:

a lock detection block generating a lock detection signal indicating whether said

output clock signal is locked to said input reference signal;

an out-of-lock detection block generating an out-of-lock signal indicating whether said output clock signal is out-of-lock with said input reference signal; and

lock generation block receiving said lock detection signal and said out-of-lock detection signal on separate paths, said lock generation block generating said lock signal based on both of said lock detection signal and said out-of-lock detection signal.

11. The lock generator circuit of claim 10, further comprising:

a phase frequency detector generating an up signal and a down signal, wherein said up signal indicates that the frequency of said output clock signal is to be increased and said down signal indicates that the frequency of the said output clock signal is to be reduced to lock said output clock signal to said input reference clock signal,

wherein each of said lock detection block and said out-of-lock detection block respectively generate said lock detection signal and said out-of-lock detection block based on said up signal and said down signal.

12. The lock generator circuit of claim 10, wherein said lock generation block further comprises:

a counter counting a number of lock detection signals indicating a lock when said lock signal indicates that said output clock signal is not locked, said lock detection signals being generated by said lock detection circuit, said counter being reset to a lower value if a lock detection signal indicates that said output clock signal is not locked, wherein said lock signal is asserted to indicate a lock when said counter at least equals a pre-specified number.

13. The lock generator circuit of claim 12, further comprising a multiplexor receiving said lock detection signal and said out-of-lock detection signal, said multiplexor forwarding said lock detection signal only when said lock signal indicates that said output clock signal is locked and forwarding said out-of-lock detection signal otherwise, the output of said multiplexor being connected to a reset input of said counter.

14. A system comprising:

an application block driven by an output clock signal; and

a signal generation circuit generating said output clock signal synchronized with an input reference signal, said signal generation block comprises:

a PLL generating said output clock signal; and

a PLL lock generator generating a lock signal representing whether said output clock signal is locked to said input reference signal, wherein said output clock signal is provided to said application block only if said lock signal indicates that said output clock signal is locked to said input reference signal, said PLL lock generator comprising:

a lock detection block generating a lock detection signal indicating whether said output clock signal is locked to said input reference signal;

an out-of-lock detection block generating an out-of-lock signal indicating whether said output clock signal is out-of-lock with said input reference signal; and

a lock generation block receiving both said lock detection signal and

said out-of-lock detection signal, said lock generation block generating said lock signal based on both of said lock detection signal and said out-of-lock detection signal.

15. The system of claim 14, wherein said PLL lock generator further comprises:

a first phase frequency detector (PFD) generating an up signal and a down signal, wherein said up signal indicates that the frequency of said output clock signal is to be increased and said down signal indicates that the frequency of the said output clock signal is to be reduced to lock said output clock signal to said input reference clock signal,

wherein each of said lock detection block and said out-of-lock detection block respectively generate said lock detection signal and said out-of-lock detection block based on said up signal and said down signal.

16. The system of claim 15, wherein said PLL comprises a second PFD for generating another up signal and another down signal.

17. The system of claim 14, wherein said lock detection circuit comprises:

a first sampling circuit receiving an up signal as an input and being clocked by a down signal, wherein said up signal indicates that the frequency of said output clock signal is to be increased and said down signal indicates that the frequency of the said output clock signal is to be reduced to lock said output clock signal to said input reference clock signal, said first sampling circuit generating a first output;

a second sampling circuit receiving said down signal as an input and being clocked

by said up signal, said second sampling circuit generating a second output; and

an examining circuit receiving said first output and said second output, and generating a signal indicating that said output clock signal is locked to said input reference signal if both said first output and said second output are at a logical low level.

18. The system of claim 15, wherein said examining circuit comprises:

a NOR gate;

a first delay element placed before either a data input or a clock input of said first sampling circuit; and

a second delay element placed before either a data input or a clock input of said second sampling circuit.

19. The system of claim 18, wherein said examining circuit further comprises:

a plurality of flip-flops cascaded in series;

a first one of said plurality of flip-flops receiving said signal generated by said examining circuit as input, and wherein said plurality of flip-flops are clocked by an output of one of said first delay element and said second delay element; and

an OR gate generating an output by performing a logical OR operation on the outputs of said plurality of flip-flops cascaded in series,

wherein said output of said OR gate represents a jitter free indication of whether said output clock signal is locked to said input reference signal.

20. The system of claim 19, wherein said plurality of flip-flops cascaded in series are

clocked by a delayed signal generated by either said first delay element or said second delay element.

21. The system of claim 14, wherein said out-of-lock detection circuit comprises:

an XOR gate receiving an up signal and a down signal,

wherein said up signal indicates that the frequency of said output clock signal is to be increased and said down signal indicates that the frequency of the said output clock signal is to be reduced to lock said output clock signal to said input reference clock signal,

wherein an output of said XOR gate represents whether said output clock is out-of-lock with said input reference signal.

22. The system of claim 21, wherein said out-of-lock detection circuit further comprises:

a plurality of flip-flops cascaded in series;

a first one of said plurality of flip-flops receiving an output of said XOR gate as an input; and

a NAND gate receiving an output of each of said plurality of flip-flops,

wherein an output of said NAND gate generates a jitter free signal indicating whether said output clock signal is out-of-lock with said input reference signal.

23. The system of claim 22, wherein each of plurality of flip-flops cascaded in series is clocked by said output clock signal.

24. A system comprising:

an application block driven by an output clock signal; and

a signal generation circuit generating said output clock signal synchronized with an input reference signal, said signal generation block comprises a lock detector block for detecting whether an output clock signal is locked to an input reference signal, said lock detector block comprising:

a first sampling circuit receiving an up signal as an input and being clocked by a down signal, wherein said up signal indicates that the frequency of said output clock signal is to be increased and said down signal indicates that the frequency of the said output clock signal is to be reduced to lock said output clock signal to said input reference clock signal, said first sampling circuit generating a first output indicating whether said output clock signal is out-of-lock;

a second sampling circuit receiving said down signal as an input and being clocked by said up signal, said second sampling circuit generating a second output indicating whether said output clock signal is out-of-lock; and

an examining circuit receiving said first output and said second output, and generating a signal indicating that said output clock signal is locked to said input reference signal if both said first output and said second output indicate that said output clock signal is not out-of-lock.

25. The system of claim 24, wherein said examining circuit comprises a NOR gate, said first sampling circuit comprises a first flip-flop and said second sampling circuit comprises a second flip-flop.

26. The system of claim 25, wherein said signal generation circuit further comprising:

a first delay element placed before either a data input or a clock input of said first flip-flop; and

a second delay element placed before either a data input or a clock input of said second flip-flop.

27. The system of claim 26, further comprises:

a plurality of flip-flops cascaded in series;

a first one of said plurality of flip-flops receiving said signal generated by said examining circuit as input, and wherein said plurality of flip-flops are clocked by an output of one of said first delay element and said second delay element; and

an OR gate generating an output by performing a logical OR operation on the outputs of said plurality of flip-flops cascaded in series,

wherein said output of said OR gate represents a jitter free indication of whether said output clock signal is locked to said input reference signal.

28. The lock detector block of claim 27, wherein said plurality of flip-flops cascaded in series are clocked by a delayed signal generated by either said first delay element or said second delay element.

29. A lock detector block for detecting whether an output clock signal is locked to an input reference signal, said lock detector block comprising:

means for receiving an up signal and a down signal, wherein said up signal indicates that the frequency of said output clock signal is to be increased and said down signal indicates that the frequency of the said output clock signal is to be reduced to lock said output clock signal to said input reference clock signal;

means for sampling said up signal clocked by said down signal to generate a first output;

means for sampling said down signal clocked by said up signal to generate a second output; and

means for examining said first output and said second output to generate a signal indicating that said output clock signal is locked to said input reference signal if both of said first output and said second output indicate that said output clock signal is not out-of-lock.

30. The lock detector block of claim 29, wherein each of said means for sampling said up signal and said sampling comprises a flip-flop.

31. An out-of-lock detector block for detecting whether an output clock signal is out-of-lock with an input reference signal, said out-of-lock detector block comprising:

means for receiving an up signal and a down signal,

wherein said up signal indicates that the frequency of said output clock signal is to be increased and said down signal indicates that the frequency of the said output clock signal is to be reduced to lock said output clock signal to said input reference clock signal; and

means for performing an XOR operation of said up signal and said down signal,

wherein an output of said XOR gate represents whether said output clock is out-of-

lock with said input reference signal.

32. A lock generator circuit for generating a lock signal indicating whether an output clock signal is locked to an input reference signal, said lock generator circuit comprising:

means for generating a lock detection signal indicating whether said output clock signal is locked to said input reference signal;

means for generating an out-of-lock signal indicating whether said output clock signal is out-of-lock with said input reference signal; and

means for generating said lock signal by examining said lock detection signal and said out-of-lock detection signal.

33. A method of detecting whether an output clock signal is locked to an input reference signal, said method comprising:

receiving an up signal and a down signal, wherein said up signal indicates that the frequency of said output clock signal is to be increased and said down signal indicates that the frequency of the said output clock signal is to be reduced to lock said output clock signal to said input reference clock signal;

sampling said up signal clocked by said down signal to generate a first output;

sampling said down signal clocked by said up signal to generate a second output; and

examining said first output and said second output to generate a signal indicating that said output clock signal is locked to said input reference signal if both of said first output and said second output indicate that said output clock signal is not out-of-lock.

34. The method of claim 33, wherein each of said sampling said up signal and said sampling said down signal is performed using a flip-flop.

35. A method of detecting whether an output clock signal is out-of-lock with an input reference signal, said method comprising:

receiving an up signal and a down signal,

wherein said up signal indicates that the frequency of said output clock signal is to be increased and said down signal indicates that the frequency of the said output clock signal is to be reduced to lock said output clock signal to said input reference clock signal; and

performing an XOR operation of said up signal and said down signal,

wherein an output of said XOR gate represents whether said output clock is out-of-lock with said input reference signal.

36. A method of generating a lock signal indicating whether an output clock signal is locked to an input reference signal, said method comprising:

generating a lock detection signal indicating whether said output clock signal is locked to said input reference signal;

generating an out-of-lock signal indicating whether said output clock signal is out-of-lock with said input reference signal; and

generating said lock signal by examining said lock detection signal and said out-of-lock detection signal.